REMARKS/ARGUMENTS

Claims 1-5, 7-14 and 16-22 are pending in the application. Reconsideration in view the following remarks is respectfully requested.

The Office Action rejects claims 13-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Yeager et al. (U.S. Patent No. 5,758,112). Applicants again gratefully acknowledge Examiner's allowance of claims 1-5, 7 and 19-22.

Applicants respectfully submit the Yeager reference does not teach suggest or disclose "[a] method for recovering registers in a processor, comprising: reading a bit in an active list; reclaiming a physical register from a new field of said active list to a free list according to said bit; and setting said bit during a misprediction condition" (e.g., as disclosed in the embodiment of claim 13).

The Office Action states that Yeager teaches a method for recovering registers in a processor (col. 2, lines 40-42); reading a bit in an active list (col. 15, line 61 to col. 16, line 14); reclaiming a physical register from said active list to a free list according to said bit (col. 16, lines 1-14). Column 2, lines 40-42 state:

> The present invention offers a highly efficient mechanism for saving and restoring register-renaming information to facilitate branch prediction and speculative execution.

The cited section of Yeager does not disclose at least a misprediction condition as specifically recited in the embodiment of claim 1.

Column 15, lines 61-67 state:

> Done bit 286 and exception bit 288, as shown in FIG. 2, are initialized, usually to zero, when an instruction is decoded. These bits are set when an instruction completes execution. The "done" and "exception" bits control when instructions graduate. When "done," up to four instructions can graduate per cycle, provided no previous instruction had an exception.

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The cited section discloses the "done" and "exception" bits of Yaeger, but again does not disclose a "misprediction condition", or any equivalent thereof, as specifically recited in the embodiment of claim 13.

Column 16 lines 1-14 state:

> Instructions graduate in original program order from active list 212, after they have been completed by a functional unit. Instructions complete (i.e., become eligible for graduation) when their results have been computed and stored in a register. Because execution and completion can occur out of order, each completion is recorded by setting done bit 286 for that instruction. Address queue 308 generates "done" signals for load and store instructions. For all other instructions, an execution unit sets the done bit of an instruction in active list 212. As instructions graduate, a "graduation unit" (not shown) removes instructions from active list 212 and appends their old destination registers to free lists 208 or 210 for re-use. Up to four instructions can graduate in parallel during each cycle.

The cited section discloses the utility and operation of the "done bit" of Yeager, but fails to disclose a "misprediction condition" or any equivalent thereof. Therefore, since each and every limitations of claim 13 is not taught by the Yeager reference, the 35 U.S.C. 102(b) rejection should be withdrawn and claim 13 should be allowed. Claims 14 and 16-18 are allowable for depending from an allowable base claim.

For at least the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

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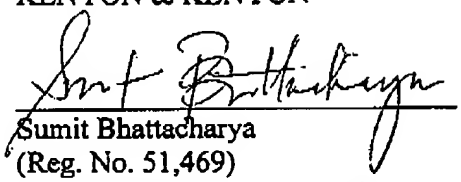
The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments to Deposit Account No. **11-0600**.

Respectfully submitted,

KENYON & KENYON

Dated: November 18, 2005 By: 

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